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10EC/TE71

Seventh Semester B.E. Degree Examination, June/July 2018
Computer Communication Networks

Time: 3 hrs.

Max. Marks:100

Note: Answer any FIVE full questions, selecting atleast TWO questions from each part.

PART – A

- 1
 - a. Match the following functions to the appropriate layers in the OSI model :
 - i) Reliable process – to – process message delivery.
 - ii) Route selection.
 - iii) Dividing the transmitted bit stream into frames.
 - iv) Provides user services such e-mail and File transfer.
 - v) Transmission of bit stream across physical medium. (05 Marks)
 - b. Give a brief over of SS7 signaling. (05 Marks)
 - c. With diagram, explain TCP / IP protocol stack. (06 Marks)
 - d. Calculate the minimum time required to download 0.5 million bytes of information using of the following technologies :
 - i) V 32 modem ii) V 90 modem iii) ADSL modem iv) Cable modem. (04 Marks)
- 2
 - a. What is Framing? How frames can be classified? Explain bit stuffing and destuffing with an example. (10 Marks)
 - b. With necessary figures, explain the stop and wait ARQ protocol for noisy channels. (10 Marks)
- 3
 - a. Explain CSMA and show the behaviour of the three persistence methods of CSMA. Compare the vulnerable times in CSMA and CSMA/CD. (10 Marks)
 - b. A slotted ALOHA network transmits 500 bit frames using a shared channel with 500 Kbps bandwidth. Find the throughput if the system produces 500 frames / sec. (04 Marks)
 - c. Explain Polling & token passing in controlled access method. (06 Marks)
- 4
 - a. Give the four generation of Ethernet and their data rates. (04 Marks)
 - b. Explain the following with respect to Fast Ethernet :
 - i) Implementation ii) Encoding iii) 100 – BASE – TX. (06 Marks)
 - c. What is Hidden station and exposed station problem? How it can be solved? (10 Marks)

PART – B

- 5
 - a. Explain each of the following in brief :
 - i) Passive hub ii) Repeater iii) Bridge iv) Router. (08 Marks)
 - b. What are Transparent bridges? Explain the process of learning in transparent bridges. Which factors create looping problems in Transparent bridge. (08 Marks)
 - c. Briefly explain VLAN. (04 Marks)
- 6
 - a. What is Class less addressing in IP V₄? What is Mask? Explain. (06 Marks)
 - b. What are different strategies used in the transition of IP V₄ to IP V₆? (09 Marks)

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c. Find the error if any, in the following IP V₄ addresses :

- i) 324.74.31.12 ii) 201.14.7.24.3 iii) 10001.23.14.67
iv) 24.211.045.71 v) 221.218.44

(05 Marks)

7 a. Compare IP V4 and IP V6 headers. (04 Marks)

b. List and explain three forwarding techniques (06 Marks)

c. With necessary diagram, explain Path Vector Routing (PVR) protocol. (10 Marks)

8 a. List the TCP features. Explain TCP segment format with diagram. (10 Marks)

b. With diagram, explain Recursive and Iterative resolution. (10 Marks)

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10EC/TE72

Seventh Semester B.E. Degree Examination, June/July 2018
Optical Fiber Communication

Time: 3 hrs.

Max. Marks:100

**Note: Answer any FIVE full questions, selecting
atleast TWO questions from each part.**

PART – A

- 1
 - a. Using Snell's law, derive an expression for numerical aperture of a fiber optic cable. (08 Marks)
 - b. Explain total internal reflection and photonic crystal fibers. (06 Marks)
 - c. A graded index fiber has a core with a parabolic refractive index profile which has a diameter of 50 μm . The fiber has a numerical aperture of 0.2. Find total number of guided modes propagating in the fiber when it is operating at a wavelength of 1 μm . (06 Marks)
- 2
 - a. Derive an expression for pulse spreading due to material dispersion. (08 Marks)
 - b. Explain fiber bending loss with neat diagram. (08 Marks)
 - c. A 6 km optical link consists of multimode step index fiber with a core refractive index of 1.5 and a relative refractive index difference of 1%. Estimate the delay between the slowest and fastest modes at the fiber output and also find the rms pulse broadening due to intermodal dispersion on the link. (04 Marks)
- 3
 - a. A double-heterojunction InGaAsP LED emitting at a peak wavelength of 1310 nm has radioactive and non radioactive recombination times of 30 and 100 ns, the derive current is 40 mA. Find the recombination life time and internal power generated. (06 Marks)
 - b. Explain the GaAs homojunction injection laser with fabry-perot cavity and also derive its quantum efficiency of the above laser. (08 Marks)
 - c. A photodiode has a quantum efficiency of 65% when photons of energy 1.5×10^{-19} J are incident upon it. At what wavelength is photo diode operating and also calculate the incident power required to obtain a photo current of 2.5 μA (Assume $e = 1.602 \times 10^{-19}$). (06 Marks)
- 4
 - a. Explain the three types of misalignment which occur when joining optical fibers. (08 Marks)
 - b. Discuss about star coupler and also give its splitting and excess loss. (06 Marks)
 - c. An optical fiber has a core refractive index of 1.5. Two lengths of the fiber with smooth and perpendicular end faces are butted together. Assuming fiber axes are perfectly aligned, calculate optical loss in decibels at the joint. When there is a small air gap between the fiber end faces. (06 Marks)

PART – B

- 5
 - a. Derive SNR for Analog receiver. (08 Marks)
 - b. Explain the term receiver sensitivity. Derive an equation for receiver sensitivity interms of photodetector noise. (08 Marks)
 - c. Explain the basic sections of an optical receiver with neat diagram. (04 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
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- 6 a. Derive an expression for carrier to noise ratio of an analog optical fiber communication. (08 Marks)
b. Explain sub-carrier multiplexing technique in detail with neat diagram. (06 Marks)
c. Explain Radio over fiber links. (06 Marks)
- 7 a. Explain the operation of a polarization independent isolator with neat diagram. (06 Marks)
b. Discuss about chromatic dispersion compensator. (06 Marks)
c. Derive an equation for path difference in a 2×2 Mach-Zehnder interferometer. (08 Marks)
- 8 a. Derive an equation for amplifier gain in semiconductor optical amplifiers. (08 Marks)
b. Explain Ultra-fast point to point transmission system using optical TDM. (08 Marks)
c. Consider an EDFA being pumped at 980 nm with a 30 mW pump power. If the gain at 1550 nm is 20 dB. Find the maximum input and output power of the amplifier. (04 Marks)

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10EC73

Seventh Semester B.E. Degree Examination, June/July 2018
Power Electronics

Time: 3 hrs.

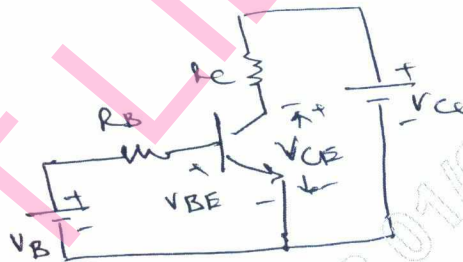
Max. Marks:100

Note: Answer any FIVE full questions, selecting atleast TWO questions from each part.

PART – A

- 1
 - a. What is a Power Converter? List the different types of power – converters and mention their conversion function. (10 Marks)
 - b. With a neat diagram and waveforms of control signal and output voltage, explain the control characteristics of IGBT and SCR. (06 Marks)
 - c. Discuss the peripheral effects of power electronics equipments. (04 Marks)
- 2
 - a. With the help of switching waveforms, explain the switching times of a power transistor. (06 Marks)
 - b. Explain how anti – saturation base drive control improves the switching performance of BJT. (06 Marks)
 - c. The beta (β) of BJT, shown in fig.Q2(c) varies from 12 to 75. The load resistance $R_C = 1.5\Omega$. The dc supply voltage $V_{CC} = 40V$ and input voltage to base circuit is $V_B = 6V$. If $V_{CE(sat)} = 1.6V$, $R_B = 0.7V$. Determine
 - i) Overdrive factor
 - ii) The forced Beta
 - iii) The power loss. (08 Marks)

Fig.Q2(c)



- 3
 - a. Explain the principle of a SCR using two transistor model. (06 Marks)
 - b. Explain the turn – on and turn – off characteristics of SCR. (08 Marks)
 - c. The latching current of a SCR inserted in between a dc voltage source of 200V and load is 100mA. Calculate the minimum width gate pulse current required to turn on this SCR in case the load consists of
 - i) $R = 20\Omega$ in series with $L = 0.2H$
 - ii) $R = 20\Omega$ in series with $L = 2.0H$. (06 Marks)
- 4
 - a. Explain briefly the half – wave controlled rectifier with RL load and derive the equation for output voltage. (08 Marks)
 - b. Explain briefly the single – phase dual converters with circuit diagram and waveform. (08 Marks)
 - c. A single phase fully controlled bridge rectifier is fed from 230V, 50Hz supply. The load is highly inductive. Find the average load voltage and current if the load resistance is 10Ω and firing angle is 45° . (04 Marks)

PART – B

- 5 a. With a neat circuit diagram and waveforms, explain the complementary commutation and derive the necessary equations. (10 Marks)
b. Draw the circuit diagram of self commutation and explain briefly with waveforms and derive equations necessary. (10 Marks)
- 6 a. What is an AC – voltage controller? With the help of waveform, explain ON – OFF controller. (06 Marks)
b. Explain the operations of a single – phase bidirectional controller with resistive load. Obtain the necessary equations and also draw the waveforms. (08 Marks)
c. A single phase full wave voltage controller has a input voltage of 230V and a load having 10Ω , i.e $R = 10\Omega$. If the firing angle is 45° , calculate the power absorbed by the load $f = 50\text{Hz}$. (06 Marks)
- 7 a. Explain the principle of operation of a step – up chopper. (06 Marks)
b. With a neat circuit diagram, explain the working of impulse commutated thyristor chopper. (08 Marks)
c. A DC chopper has a resistive load of 20Ω and input voltage 220V. When chopper is ON its voltage drop is 1.5V and chopping frequency is 10KHz. If the duty cycle is 80%, determine the average output voltage and rms output voltage and the chopper on time. (06 Marks)
- 8 a. Explain briefly the half bridge inverter with inductive load using circuit diagram and waveforms. (06 Marks)
b. Explain the performance parameters of inverters. (08 Marks)
c. Explain the variable DC link inverter with circuit diagram and waveforms. (06 Marks)

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10EC74

Seventh Semester B.E. Degree Examination, June/July 2018
Embedded System Design

Time: 3 hrs.

Max. Marks:100

**Note: Answer FIVE full questions, selecting
at least TWO questions from each part.**

PART – A

- 1 a. Compare (i) Soft real time system and Hard real time system (ii) Microprocessor and microcontroller. (04 Marks)
- b. Define embedded system and give 4 examples. With a block schematic, explain the function of the various units in a microprocessor based embedded system. (08 Marks)
- c. With a flow diagram, explain the embedded system life cycle and also distinguish between traditional and contemporary design approaches. (08 Marks)
- 2 a. Compare (i) Big Endian and Little Endian formats (ii) Truncation and Rounding of numbers (iii) Direct and Register Direct addressing. (06 Marks)
- b. Let $E = 100 \text{ VDC} \pm 1\%$, $I = 10 \text{ A} \pm 1\%$ and $R = 10 \Omega \pm 1\%$. Determine the range of power measured using three different formulae for measurement of power, using a measurement system. (06 Marks)
- c. Write the RTN model of datapath and memory interface to a microprocessor and explain the function of the registers involved. For the 4 steps in an instruction cycle, explain the function and write ISA and RTL level instruction with an example. (08 Marks)
- 3 a. With diagrams distinguish between,
 - (i) SRAM and DRAM.
 - (ii) Direct mapped and associate mapped cache memories. (08 Marks)
- b. Explain (i) DRAM write timing diagram and (ii) DRAM refresh operation. (06 Marks)
- c. Write the memory interfacing diagram to design a $4\text{K} \times 16$ bits SRAM, using $1\text{K} \times 8$ bit SRAM chips. Also write SRAM read timing diagram. (06 Marks)
- 4 a. Explain waterfall and V Life cycle models for embedded system design and development. (10 Marks)
- b. Describe the system design specification and system functional specification for a digital counter with values assumed and necessary diagrams. (10 Marks)

PART – B

- 5 a. Define the four categories of multitasking operating system, with processes and threads. (04 Marks)
- b. With a state diagram, explain the functions of the various states and also the various fields in the task control block with its diagram, in the Task management function of OS. (08 Marks)
- c. Explain (i) Reentrant code (ii) Foreground / Background system (iii) Multiple Processes and (iv) Light weight threads and Heavy weight threads. (08 Marks)
- 6 a. Compare (i) User mode and supervisor mode (ii) Programs and Processes. (04 Marks)
- b. With a diagram, explain the functions of the various layers in a high level operating system architecture. (08 Marks)
- c. Write a C code for a simple operating system Kernel which uses a shared data buffer and Task control Block for asynchronous communication of three tasks for an application. (08 Marks)

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- 7 a. Explain Amdahl's law with an equation and an example for the speed of execution. (04 Marks)
- b. Describe the time complexity analysis and Big-O notation for algorithm. (08 Marks)
- c. Analyze the selection sort algorithm for time complexity with sequence of steps and a C code for the same. (08 Marks)
- 8 a. Explain (i) Time loading (ii) Instruction counting and (iii) Preemptive scheduling. (06 Marks)
- b. Explain total memory loading with an example and formula. How individual memory loading is calculated for each area in the memory map? (06 Marks)
- c. Describe atleast 8 tricks of the trade for reducing the response time and time loading. (08 Marks)

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Seventh Semester B.E. Degree Examination, June/July 2018

DSP Algorithms and Architecture

Time: 3 hrs.

Max. Marks: 100

Note: Answer FIVE full questions, selecting at least TWO questions from each part.

PART – A

- 1 a. Explain digital signal processing with a neat block diagram. (04 Marks)
- b. Explain discrete time sequence in detail. Determine the periods for the periodic sequences ,
(i) $e^{\frac{jn\pi}{8}}$ (ii) $e^{\frac{jn3\pi}{8}}$ (08 Marks)
- c. Mention the difference between FIR and IIR filters. Find the magnitude and phase response of an FIR filter represented by the difference equation, $y(n) = 0.5x(n) - 0.5x(n-1)$ (08 Marks)
- 2 a. How does the barrel shifter in a DSP works? Explain with an example. (06 Marks)
- b. With a neat block diagram, explain the working of MAC unit. (06 Marks)
- c. Explain the bit reversed addressing mode for a 16 point FFT with a neat diagram and step by step generation of binary code. (08 Marks)
- 3 a. Compare architectural features of TMS320C25, DSP56000 and ADSP2100 fixed point DSP. (06 Marks)
- b. Explain any five addressing modes of TMS320C54XX with one example each. (10 Marks)
- c. Identify the addressing modes of the source operand in each of the following instructions:
(i) ADD, *AR2+OB, A (ii) ADD *AR2+, A (iii) ADD *AR2+%, A (iv) ADD #23h, A (04 Marks)
- 4 a. Explain the following assembler directives of TMS320 DSP processor :
(i) .mmregs (ii) .data (iii) .text (iv) .bss (04 Marks)
- b. Write a program to find the sum of series of signed number from address 410H to 41FH given by $A = \sum dmad$. (08 Marks)
- c. Explain with one example each the four types of classifications of assembly language instructions of TMS320 DSP processor. (08 Marks)

PART – B

- 5 a. Determine the values represented by the 16 bit fixed point number $N_1 = 4D00$ and $N_2 = CDCAH$ in Q7 and Q15 notation. (04 Marks)
- b. Write an ALP for the FIR filter with 200 input samples using 16 length circular buffers for the TMS320 DSP. (10 Marks)
- c. Write an ALP to multiply two Q15 numbers to produce a Q15 result for the TMS320 DSP. (06 Marks)
- 6 a. Explain scaling operation in DSP processor and derive the expression for optimal scaling factor for DIT FFT butterfly algorithm. (08 Marks)
- b. Write a pseudo code to determine 8 point DFT using DIT FFT algorithm invoking butterfly subroutine in a nested loop for each stage. (12 Marks)
- 7 a. Explain the working of DMA with respect to the TMS320 DSP processor. (08 Marks)
- b. Explain the working of interrupts in TMS320 DSP. (08 Marks)
- c. Explain the memory space organization of TMS32054XX DSP. (04 Marks)
- 8 a. Explain the working of PMC 3002 CODEC with neat block diagram. A PMC 3002 is programmed for 12 kHz sampling rate, determine the divisor N to be written to the CPLD of the DSK and various clock frequencies. (08 Marks)
- b. Explain the biotelemetry receiver system with the help of a block diagram. (06 Marks)
- c. Explain with a block diagram clipping auto correlation speech detector. (06 Marks)

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10EC/TE762

Seventh Semester B.E. Degree Examination, June/July 2018

Real Time Systems

Time: 3 hrs.

Max. Marks:100

Note: Answer FIVE full questions, selecting at least TWO questions from each part.

PART – A

- 1 a. Define Real Time Systems. How they are different from other regular systems? (06 Marks)
b. Give the classification of Real Time Systems and give suitable applications. (06 Marks)
c. Write the block diagram of a computer control system in an industry and explain its operation. (08 Marks)
- 2 a. Describe the computer control process in the following operations with the help of diagrams.
i) Sequential control ii) Loop control iii) Supervisory control. (15 Marks)
b. Explain the working principle of centralized computer control in the industry. (05 Marks)
- 3 a. What are parallel computers? Write the different architectures of parallel computer systems and explain their working principles. (08 Marks)
b. Explain with suitable diagrams the process related interfaces. (06 Marks)
c. Describe the Interrupt driven data transfer and DMA data transfer, working principles. (06 Marks)
- 4 a. Discuss the features that a real time language should possess in order to meet the real time applications. (09 Marks)
b. Explain, how the compilation of programs is carried out in the real time systems? (05 Marks)
c. Write the diagram of table driven application system and explain the working. (06 Marks)

PART – B

- 5 a. Write the block diagram of multitasking operating system and explain its functioning. (10 Marks)
b. Discuss the task priority structures employed in the real time systems. (10 Marks)
- 6 a. What is task management? Explain the total task management process in the real time systems, with the help of suitable diagrams. (12 Marks)
b. What is code sharing? How it is carried out in the multi tasking system. (08 Marks)
- 7 a. Write the typical planning phase and development phase diagrams of RTS design process and explain. (12 Marks)
b. Describe :
i) Fore ground and back ground system
ii) Semaphores. (08 Marks)
- 8 a. Discuss the i) Yourdon methodology ii) Ward and Mellor methods of RTS developments. (14 Marks)
b. Write note on Hatley and Pirbhai methodology of designing RTS. (06 Marks)

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